

FOXCONN A75M03

FAB: A1

AMD FM2 APU + FCH HUDSON D2/D3 CHIPSET

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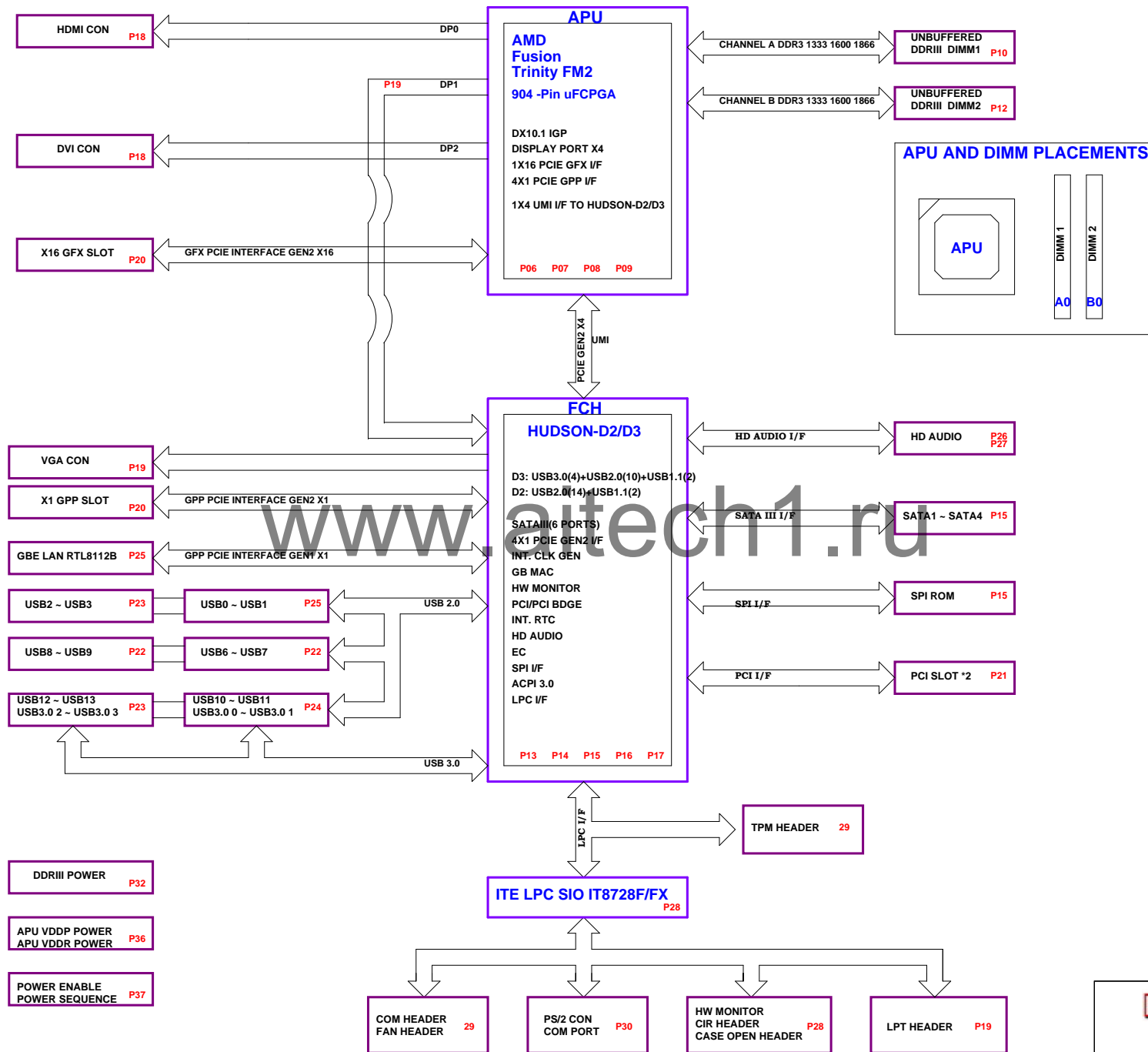
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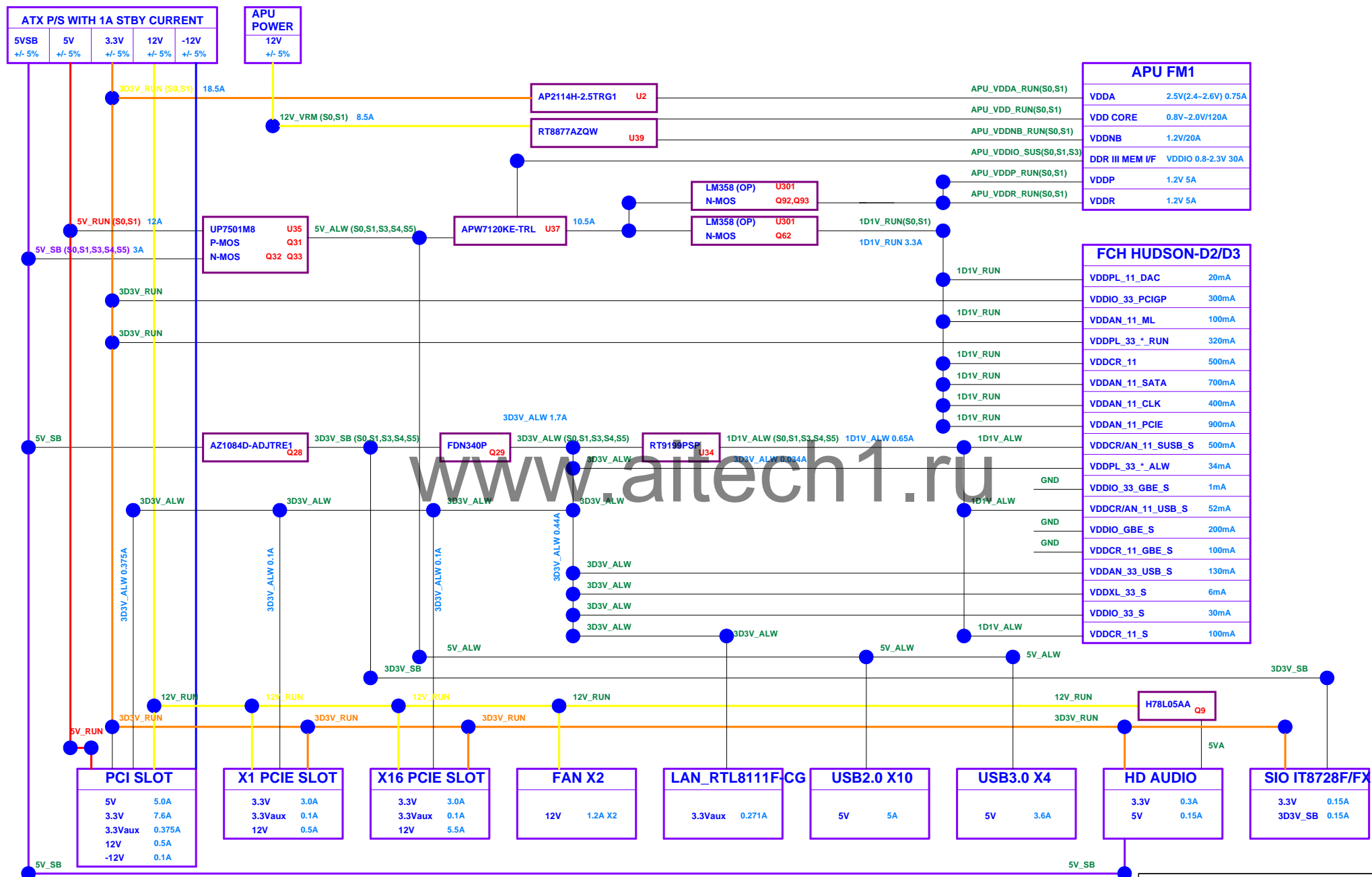
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A75M03 BLOCK DIAGRAM



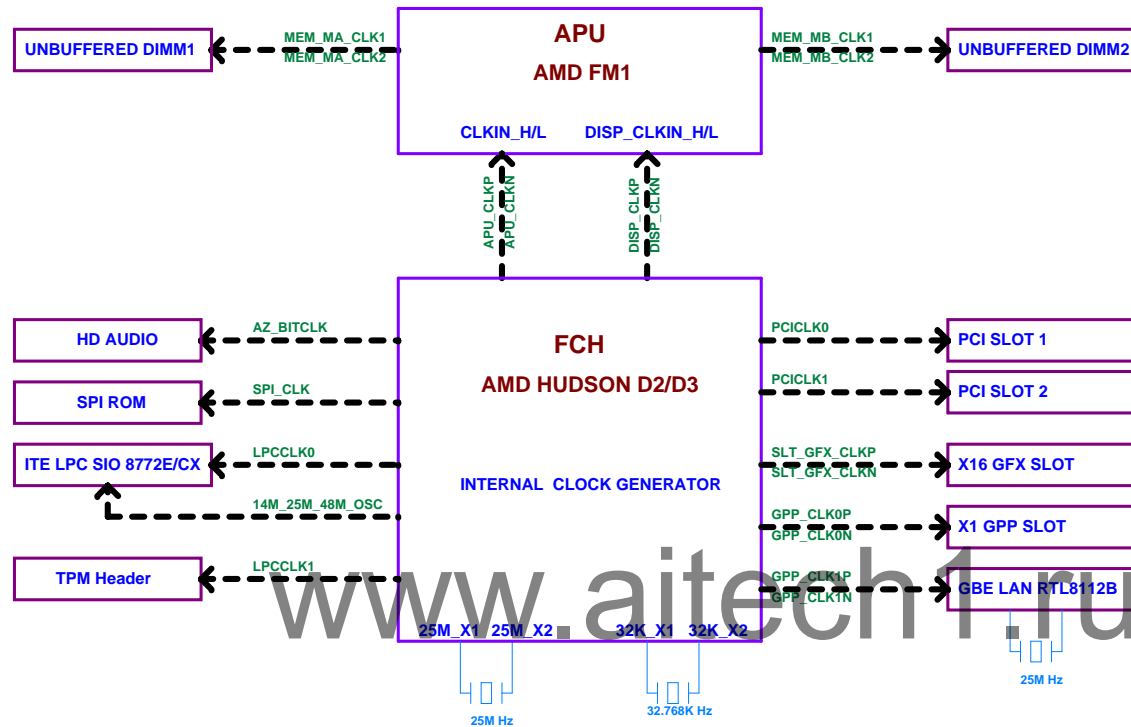
A75M03 POWER DELIVERY CHART



APU FM1	
VDDA	2.5V(2.4~2.6V) 0.7A
VDD CORE	0.8V~2.0V/120A
VDDNB	1.2V/20A
DDR III MEM I/F	VDDIO 0.8~2.3V 300mA
VDDP	1.2V 5A
VDDR	1.2V 5A

FCH HUDSON-D2/D3	
VDDPL_11_DAC	20mA
VDDIO_33_PCIGP	300mA
VDDAN_11_ML	100mA
VDDPL_33_*_RUN	320mA
VDDCR_11	500mA
VDDAN_11_SATA	700mA
VDDAN_11_CLK	400mA
VDDAN_11_PCIE	900mA
VDDCR/AN_11_SUSB_S	500mA
VDDPL_33_*_ALW	34mA
VDDIO_33_GBE_S	1mA
VDDCR/AN_11_USB_S	52mA
VDDIO_GBE_S	200mA
VDDCR_11_GBE_S	100mA
VDDAN_33_USB_S	130mA
VDDXL_33_S	6mA
VDDIO_33_S	30mA
VDDCR_11_S	100mA

A75M03 INTERNAL CLOCK MODE



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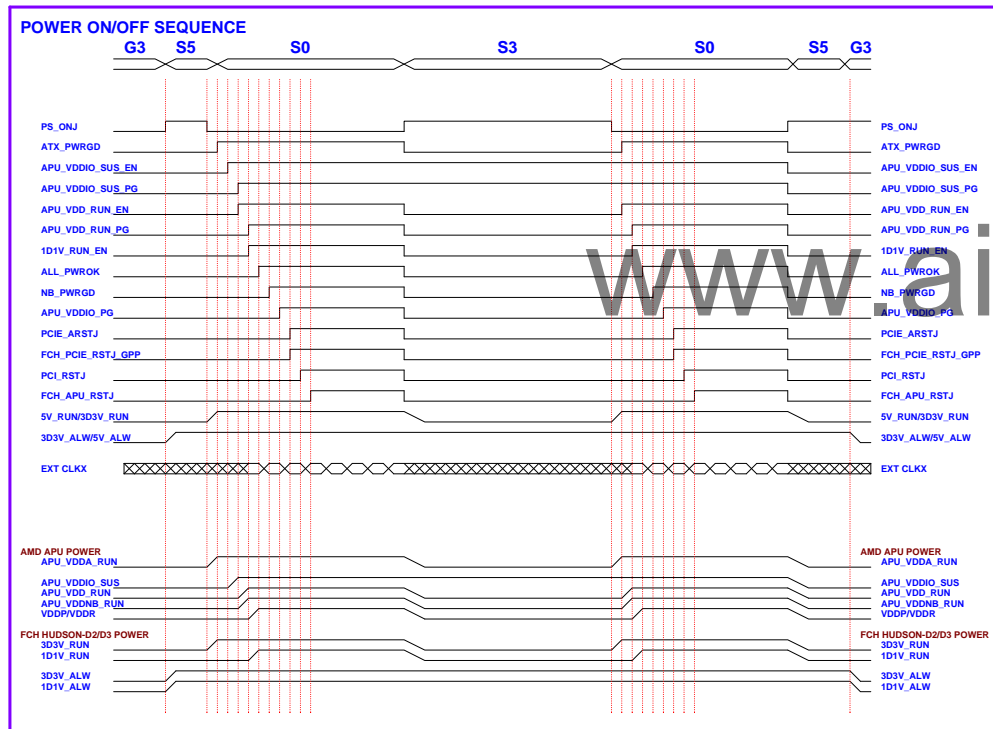
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CLOCK DISTRIBUTION			
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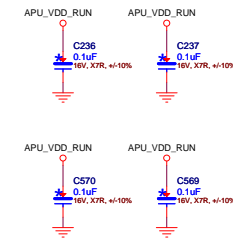
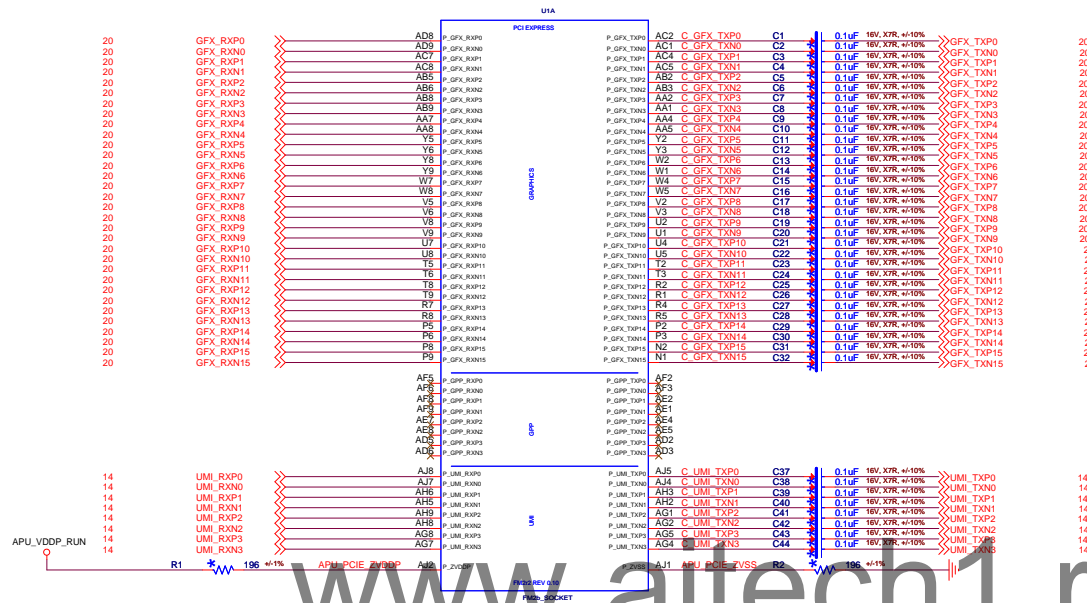
A75M03 MISC TABLES

POWER RAIL		S0	S1	S3	S4	S5	POWER RAIL		S0	S1	S3	S4	S5
12V_RUN	+12V	ON	ON	OFF	OFF	OFF	1D1V_RUN	+1.1V	ON	ON	OFF	OFF	OFF
12V_VRM	+12V	ON	ON	OFF	OFF	OFF	APU_VDD_RUN	SVI	ON	ON	OFF	OFF	OFF
N_12V_RUN	-12V	ON	ON	OFF	OFF	OFF	APU_VDDNB_RUN	SVI	ON	ON	OFF	OFF	OFF
5V_SB	+5V	ON	ON	ON	ON	ON	APU_VDDA_RUN	+2.5V	ON	ON	OFF	OFF	OFF
3D3V_SB	+3.3V	ON	ON	ON	ON	ON	APU_VDDIO_SUS	+1.5V	ON	ON	ON	OFF	OFF
5V_ALW	+5V	ON	ON	ON	ON	ON	APU_VTT_SUS	+0.75V	ON	ON	OFF	OFF	OFF
3D3V_ALW	+3.3V	ON	ON	ON	ON	ON	APU_VDDR_RUN	+1.2V	ON	ON	OFF	OFF	OFF
A_VBAT	+3.0V	ON	ON	ON	ON	ON	APU_VDDP_RUN	+1.2V	ON	ON	OFF	OFF	OFF
1D1V_ALW	+1.1V	ON	ON	ON	ON	ON							
5V_RUN	+5V	ON	ON	OFF	OFF	OFF							
3D3V_RUN	+3.3V	ON	ON	OFF	OFF	OFF							
5VA	+5V	ON	ON	OFF	OFF	OFF							

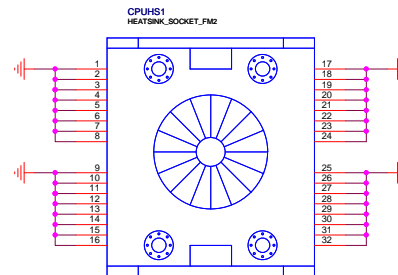
RESET TABLE		
SOURCE	SIGNAL NAME	LINKED DEVICES
FCH	PCIE_RST2J_GPP	GPP X1 SLOT/LAN RTL8112B
	FCH_PCIE_RSTJ_GPP	GFX X16 SLOT
	PCIE_ARSTJ	LPC SIO 8728E/CX /TPM
	PCI_RSTJ	PCI SLOT 0
	FCH_APU_RSTJ	APU
APU	A_HDA_RSTJ	HD AUDIO CODEC ALC662/ALC662-VD
APU	MEM_MA_RSTJ	DIMM1
APU	MEM_MB_RSTJ	DIMM2
PWR BTN	MASTER_RSTJ	FCH

Explanation	
FCH	Fusion Controller Hub
UMI	Unified Media Interface

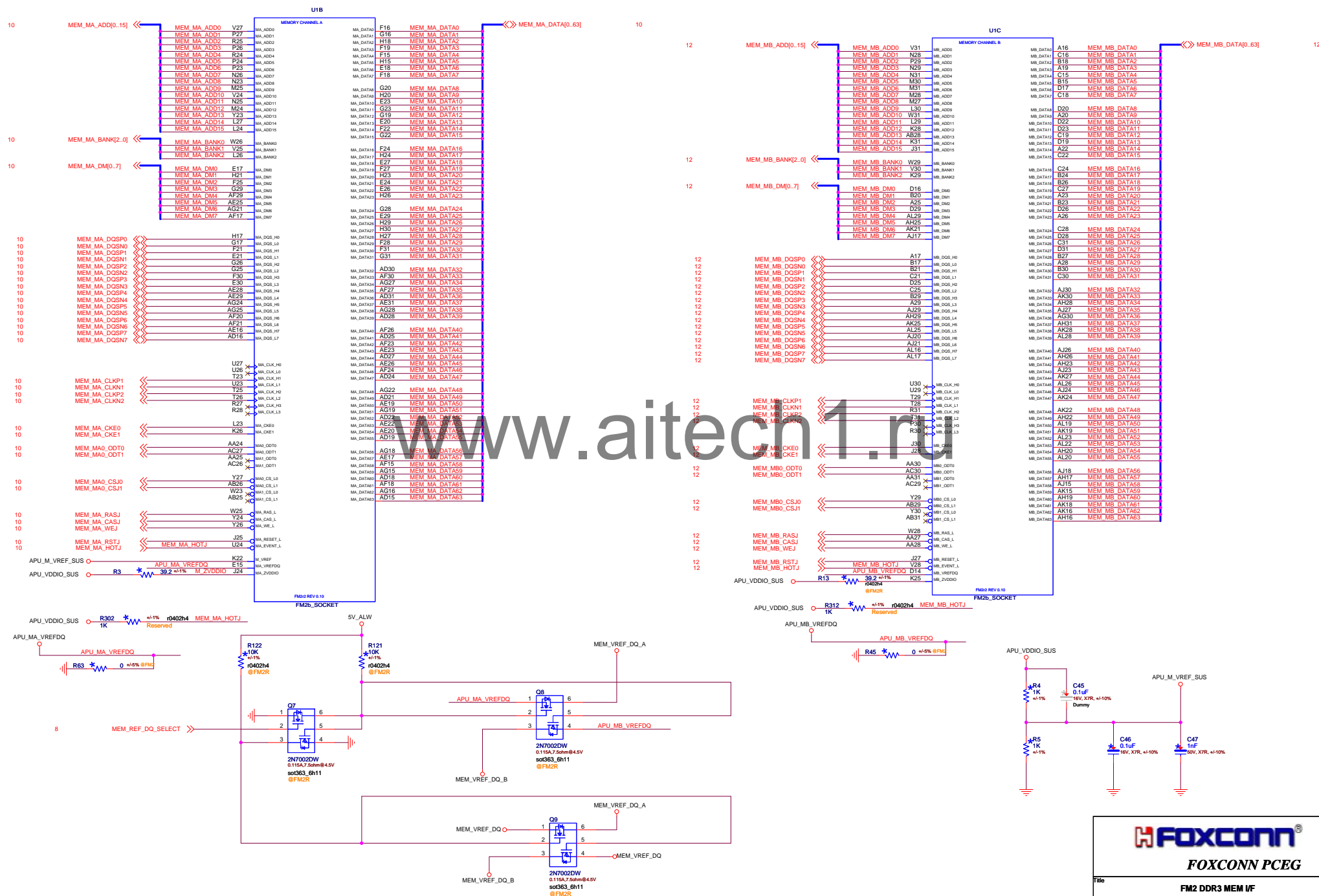




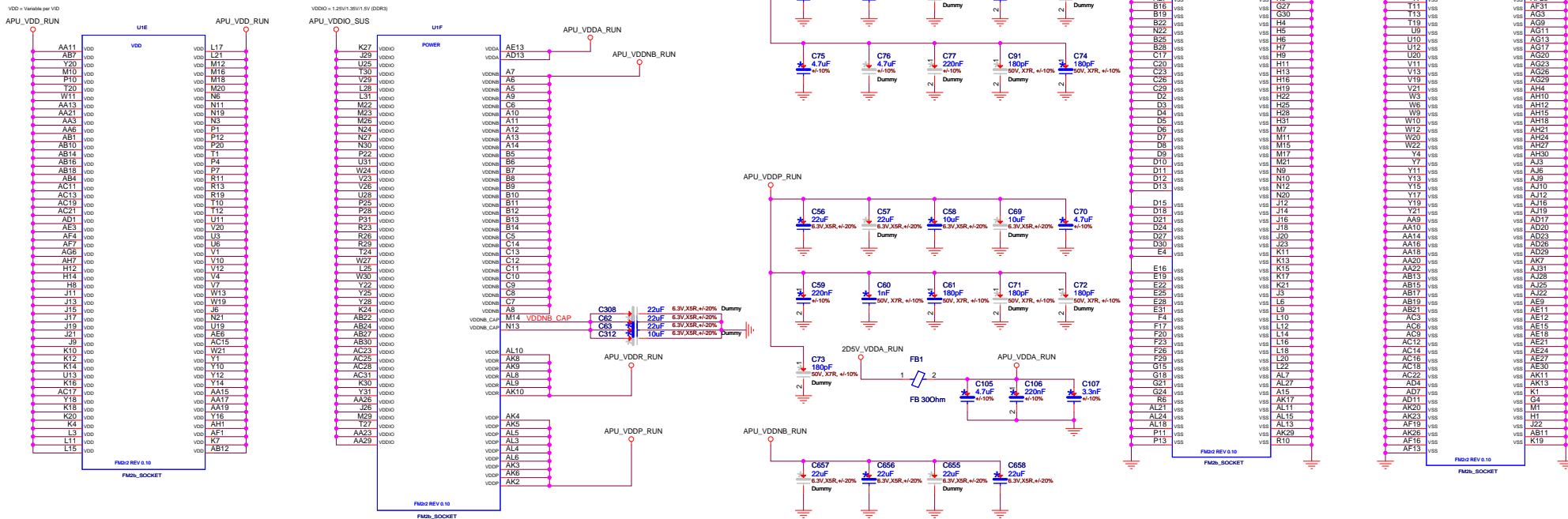
Place across each APU_VDD_RUN--GND plane seam



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PROCESSOR POWER AND GROUND

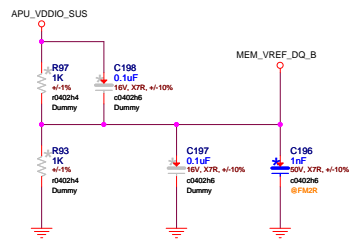


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MEM_MB_HOTJ

APU_VTT_SUS

VTT

VTT

VSS

VSS

VSS

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RSVD

ODT1

ODT0

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NC/ERR_OUT

NC/TEST4

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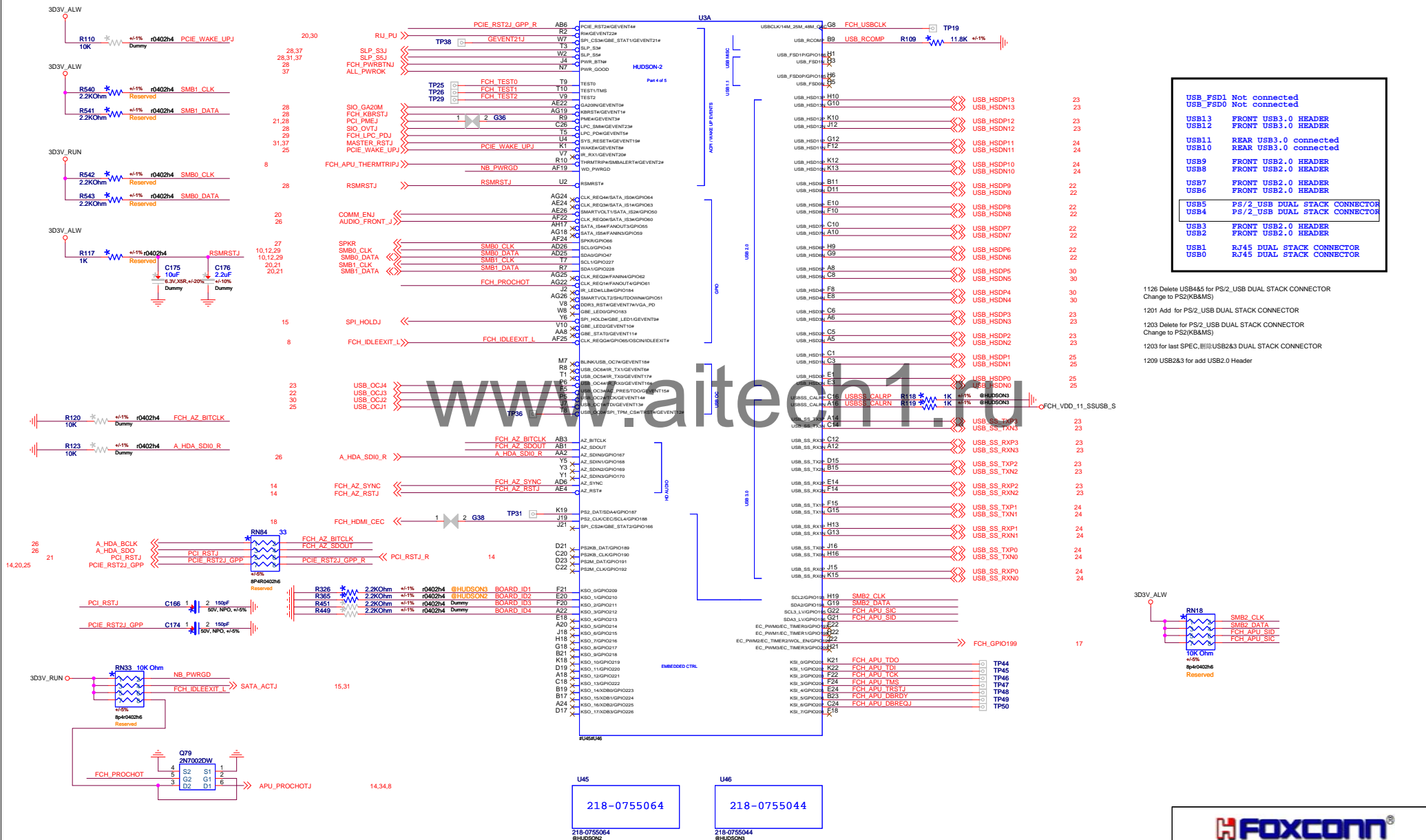
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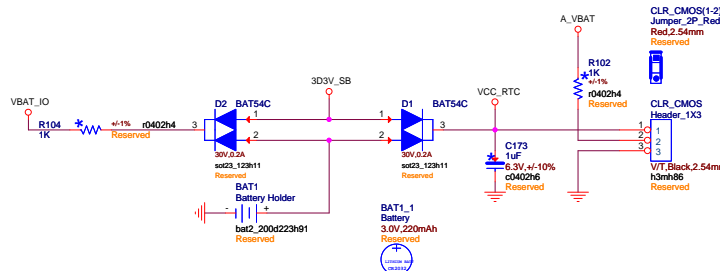
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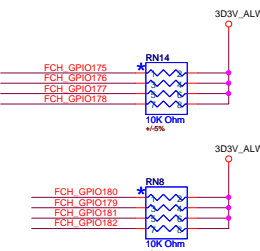
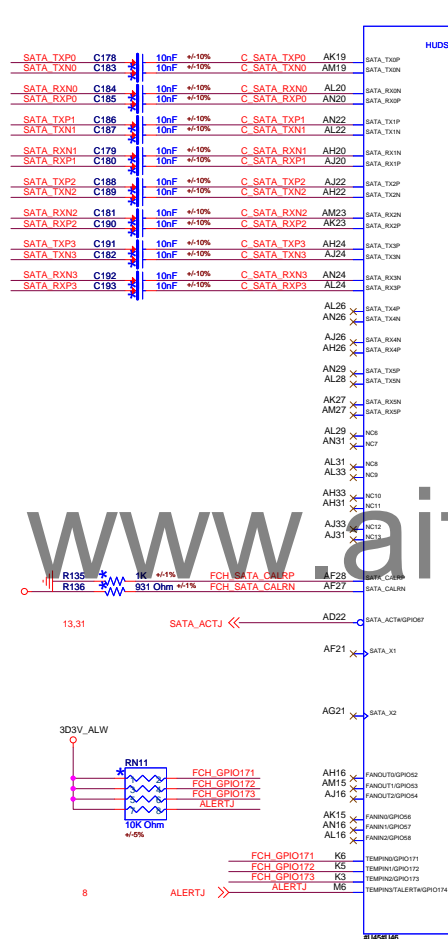
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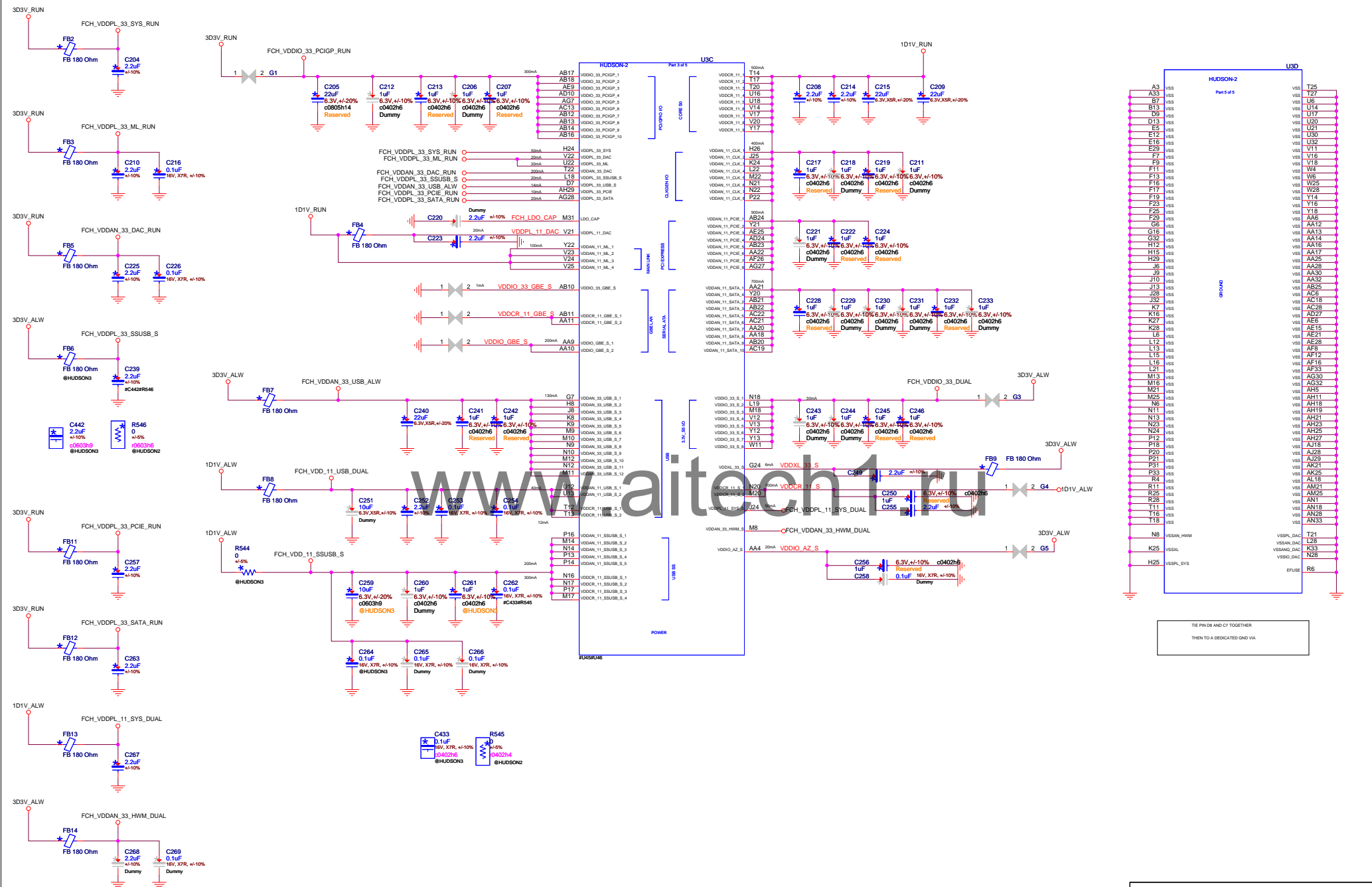
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<i>PCIE_RST2J_GPP FOR FCH PCIE DEVICE</i>	PCIE 1X / LAN
<i>PCIE_ARSTJ FOR LPC DEVICES</i>	SIO



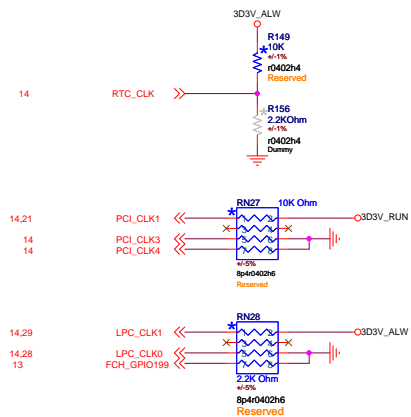


1-2: Normal
2-3: Clear COMS





TIE PIN DR AND C7 TOGETHER
THEN TO A DEDICATED GND VIA



	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	GPI0199
PULL HIGH	ALLOW PCI GEN2	USE DEBUG STRAPS	NON-FUSION APU CLOCK MODE	EC ENABLED	CLEGEN ENABLED DEFAULT	S5+ DISABLE DEFAULT	ROM TYPE: H = LPC ROM
PULL LOW	FORCE PCI GEN1 DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION APU CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLEGEN DISABLED	S5+ ENABLE	L = SPI ROM DEFAULT

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FCH DEBUG STRAPS

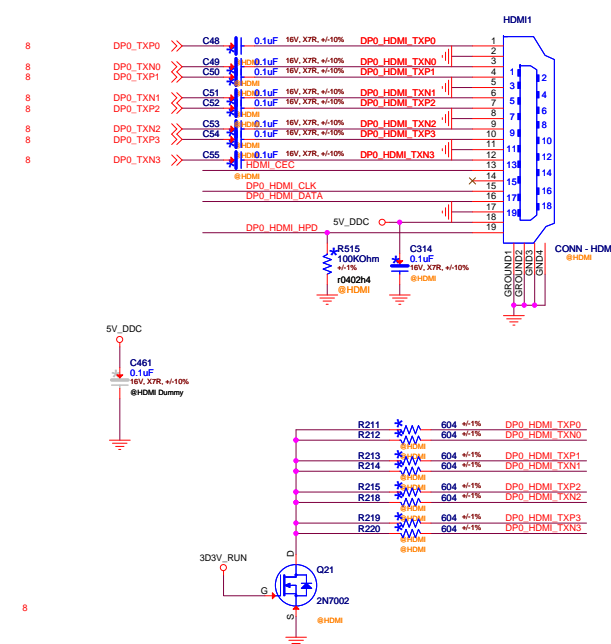
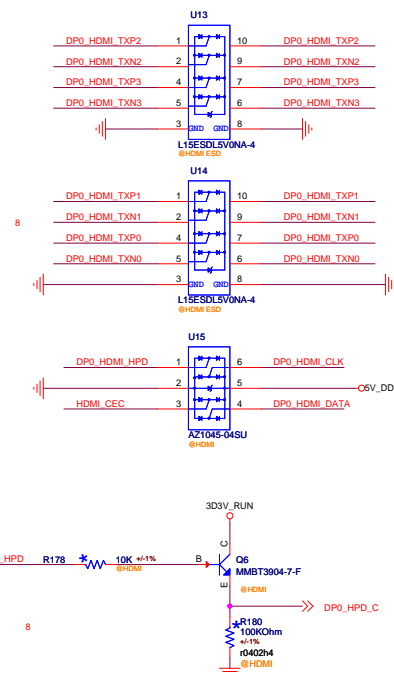
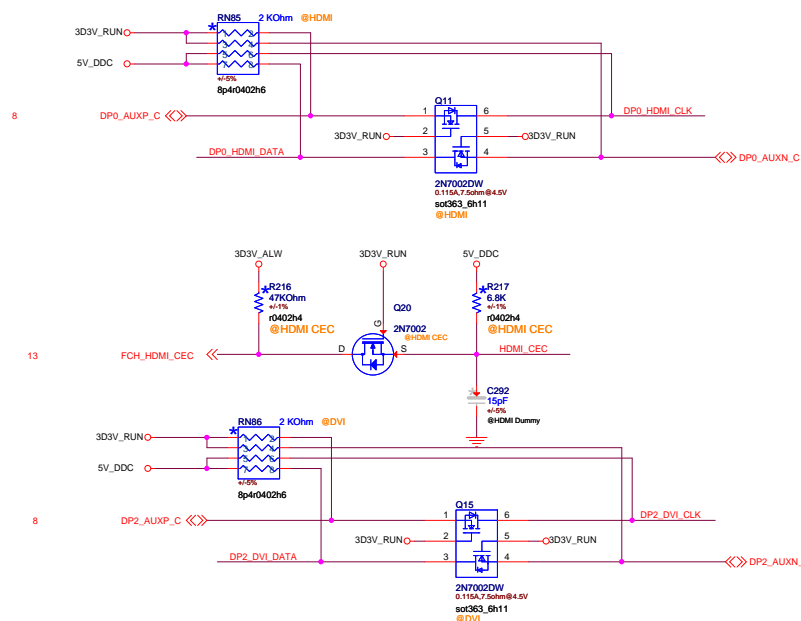
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK termination DEFAULT	USE DEFAULT PCI STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	Inverted REFCLK termination	USE EEPROM PCI STRAPS	ENABLE PCI MEM BOOT



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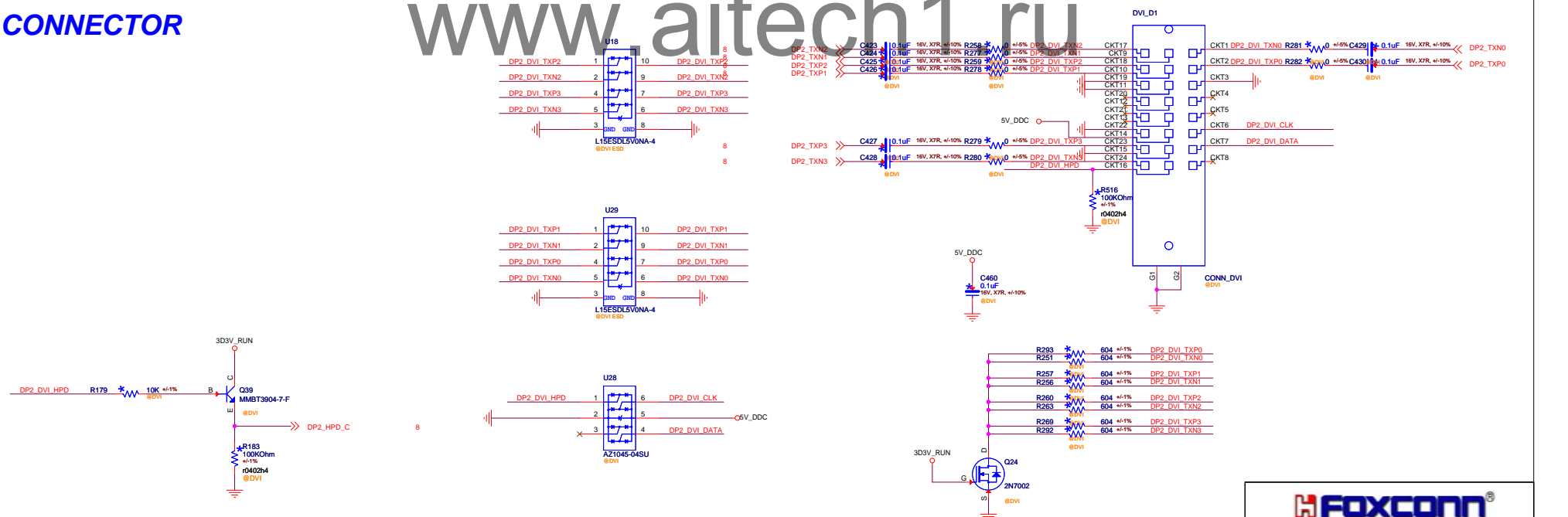
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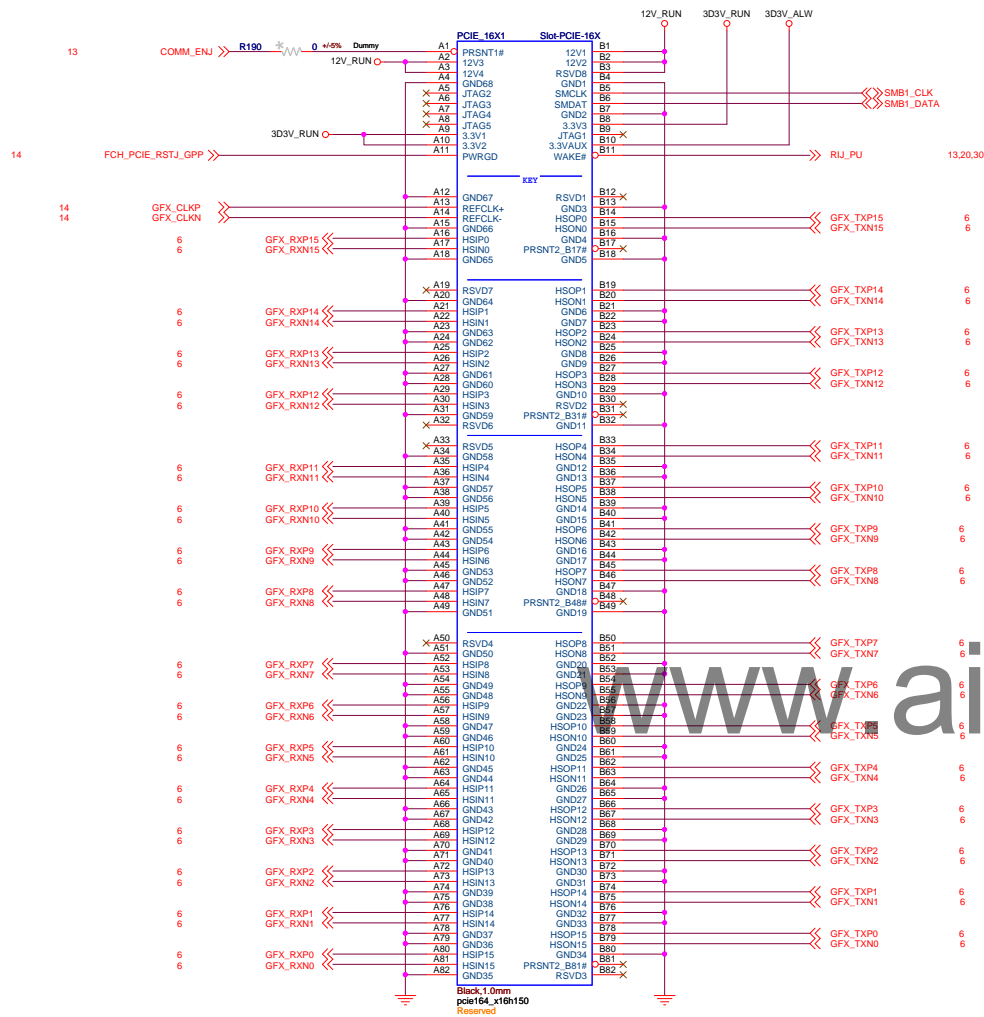
HDMI CONNECTOR



DVI CONNECTOR

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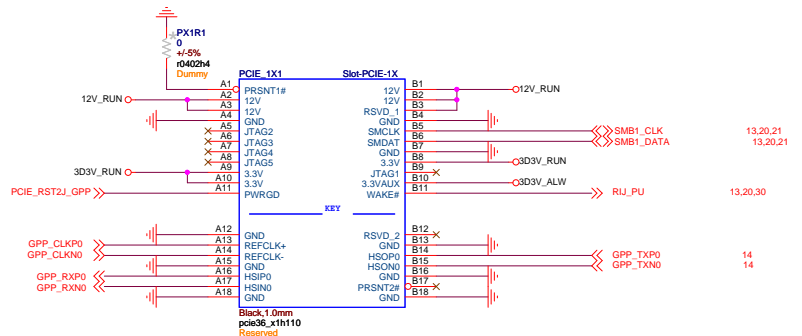
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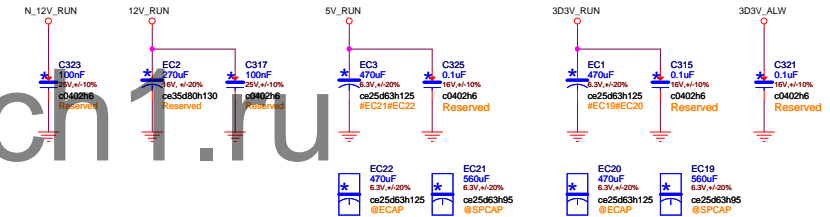
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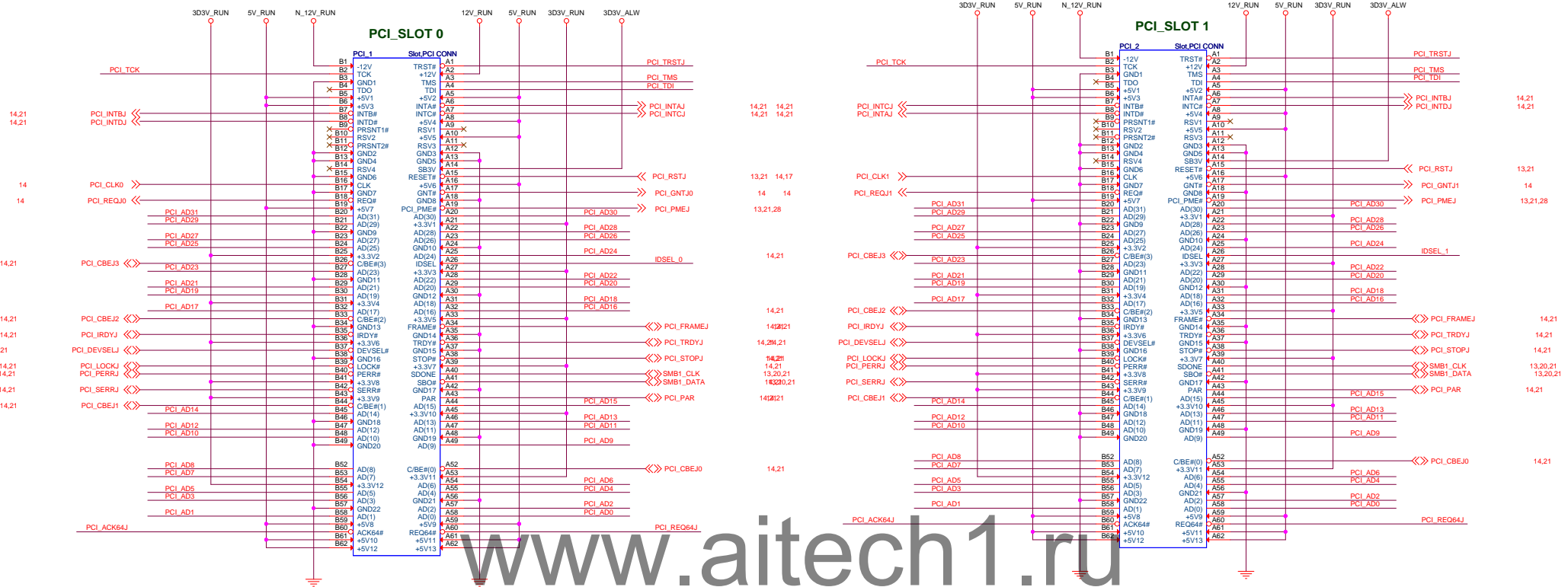
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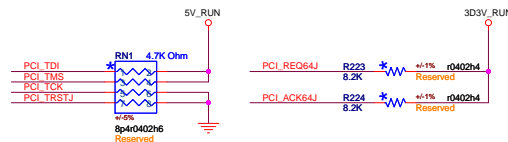
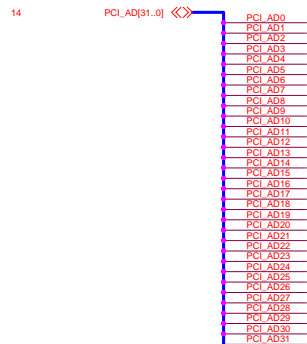
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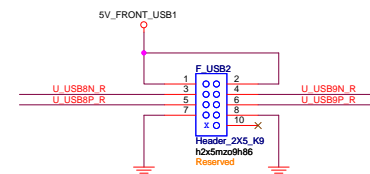
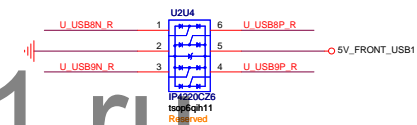
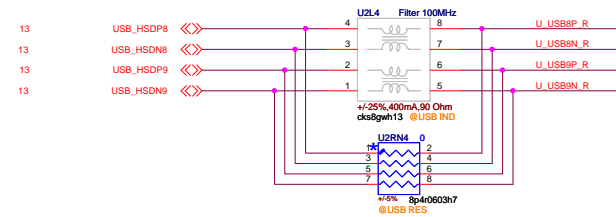
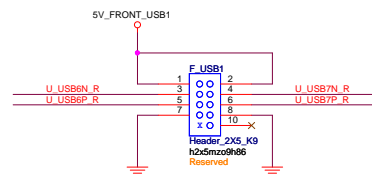
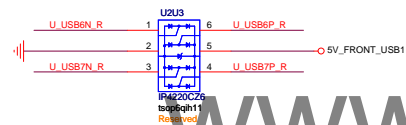
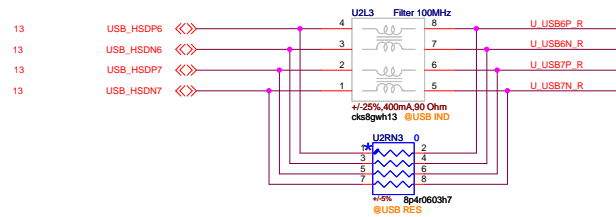
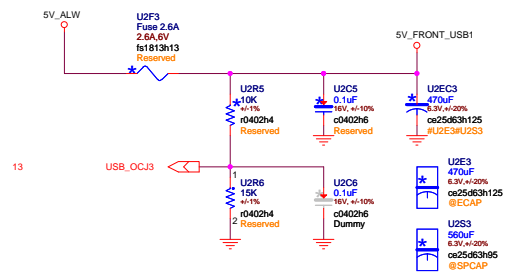


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IDSEL_0 R221 $\pm 1\%$ r0402h4 PCI_AD21
100 Ohm Reserved

IDSEL_1 R249 $\pm 1\%$ r0402h4 PCI_AD22
100 Ohm Reserved





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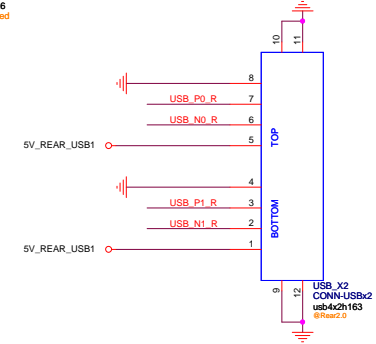
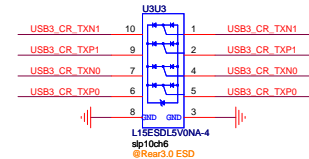
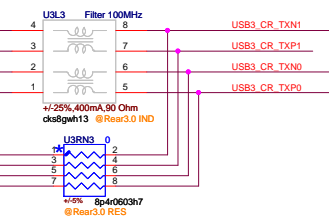
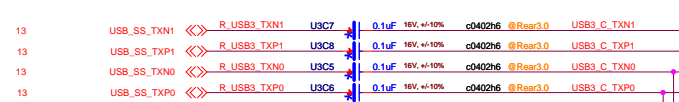
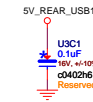
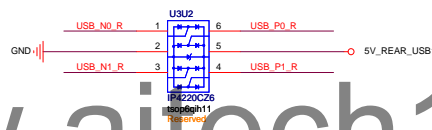
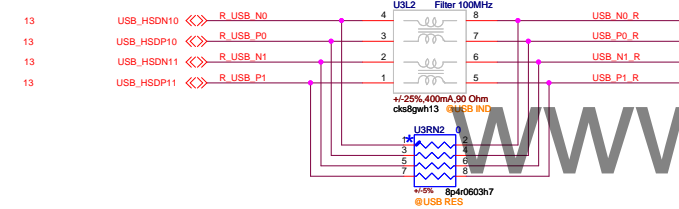
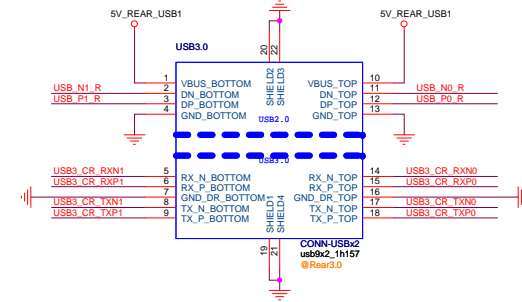
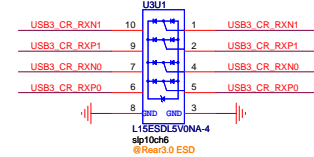
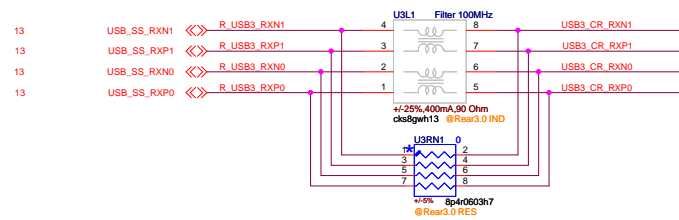
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Title: **USB2.0 FRONT HEADER**

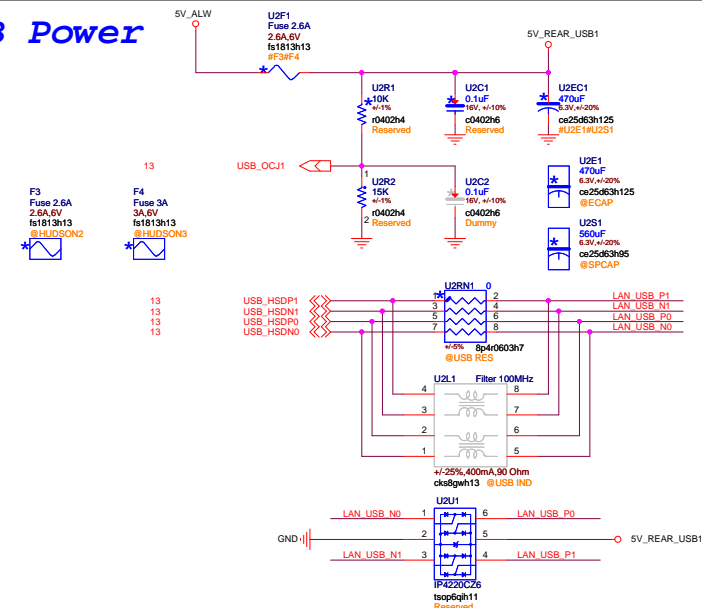
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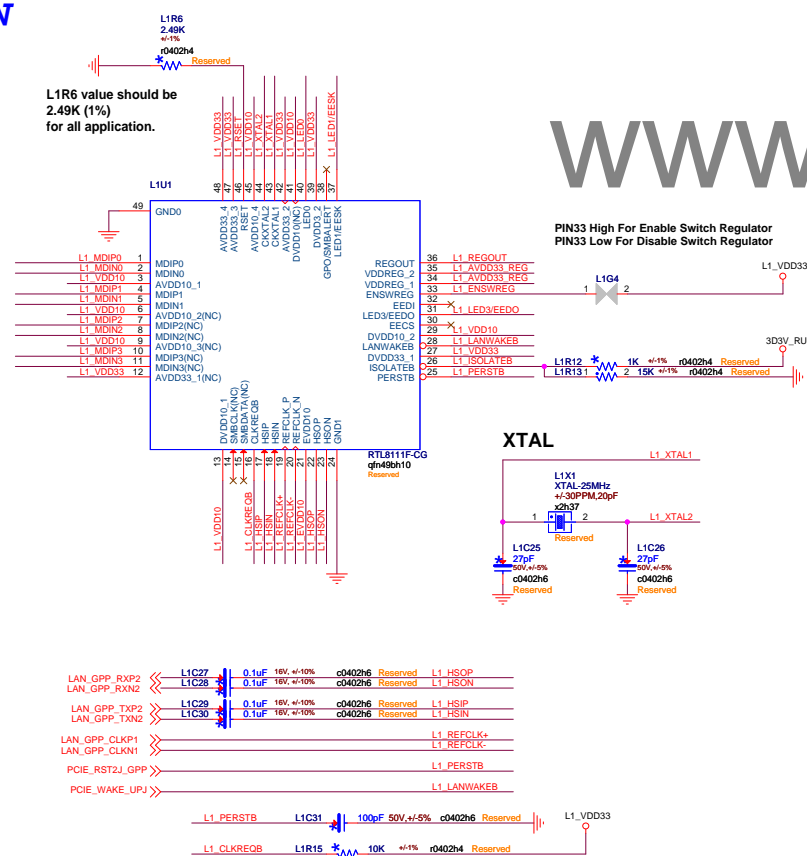




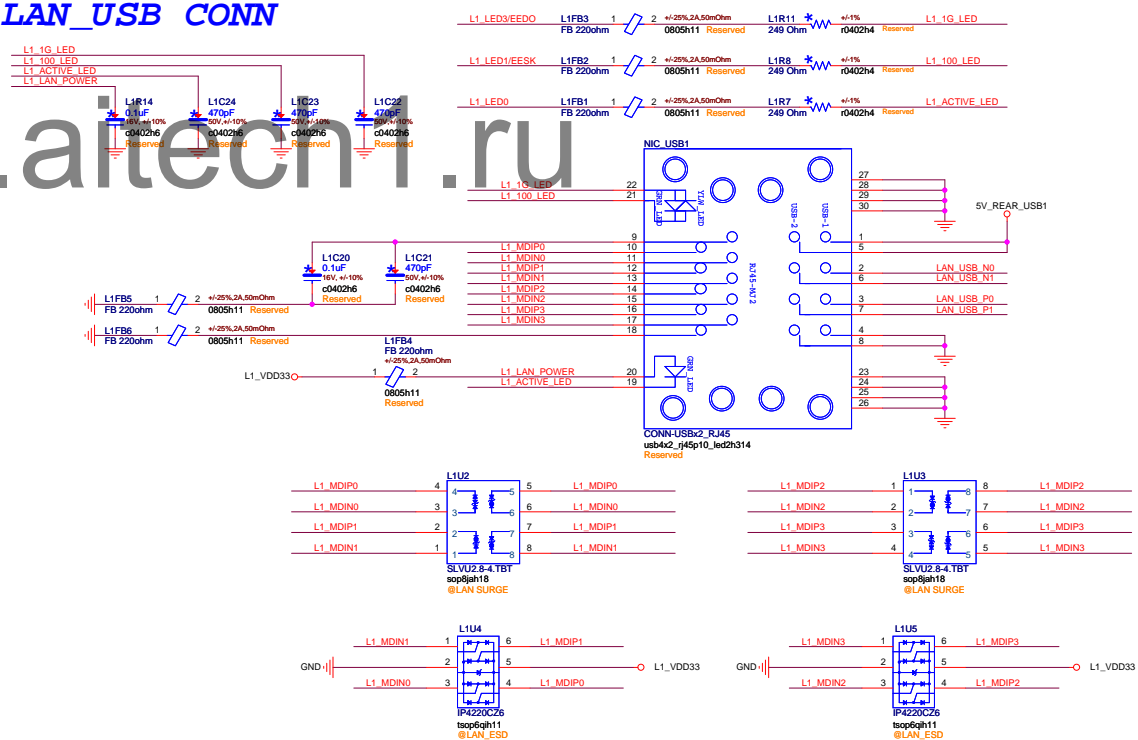
LAN



LAN

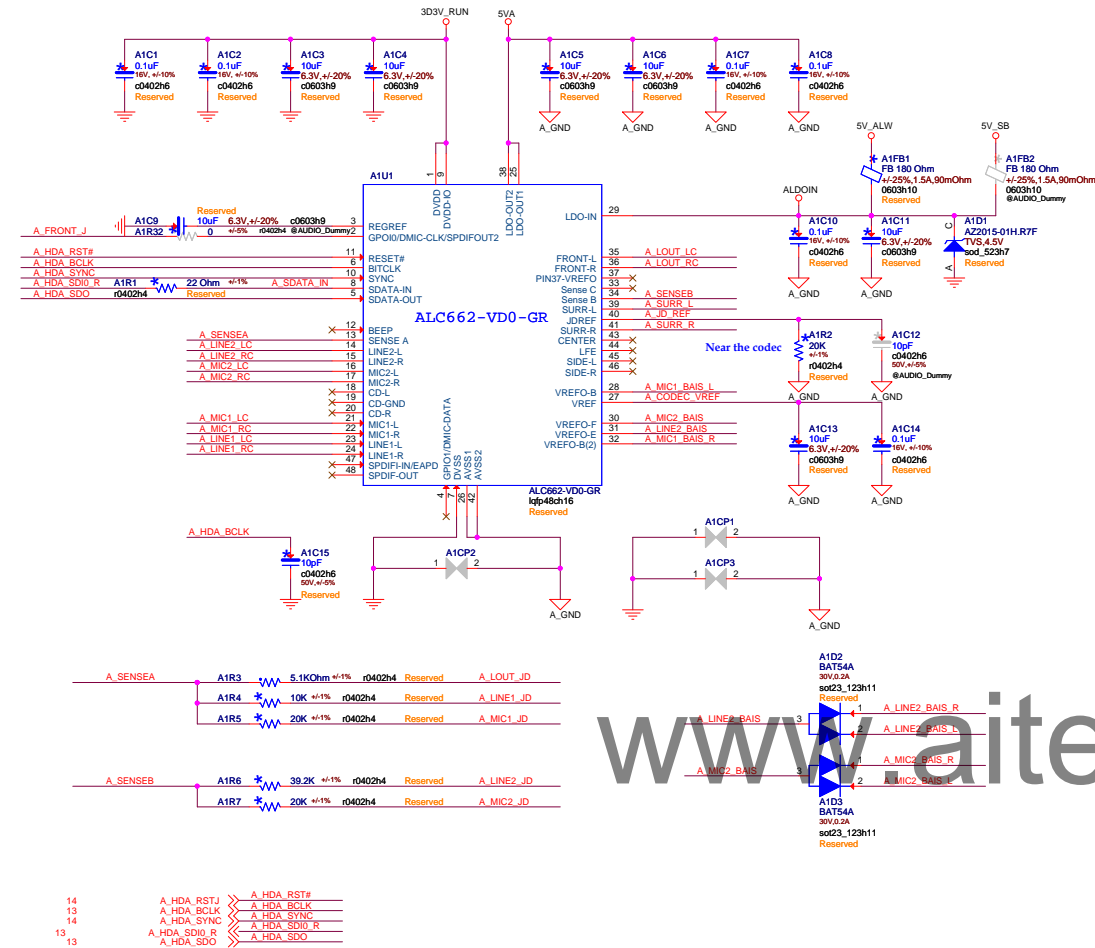


LAN USB CONN

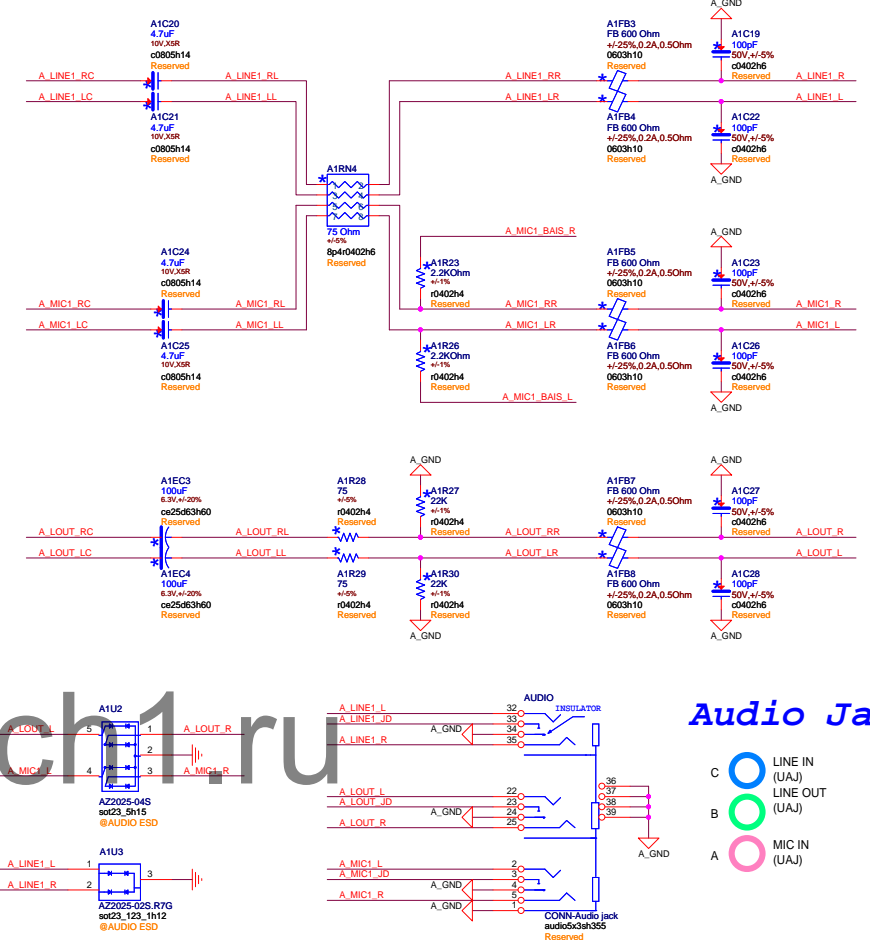


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Audio



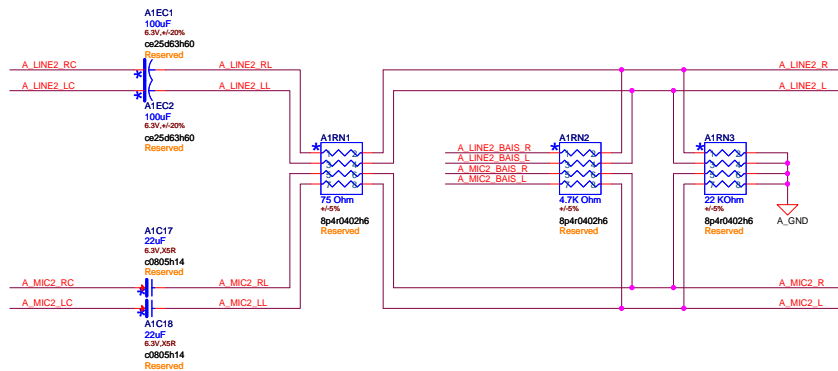
Rear Audio



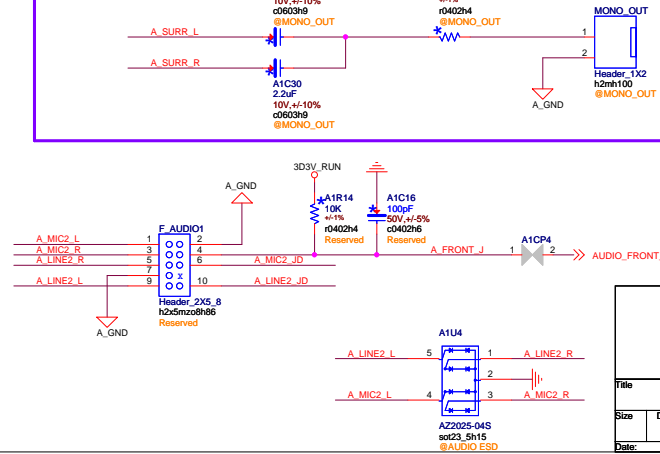
Audio Jack



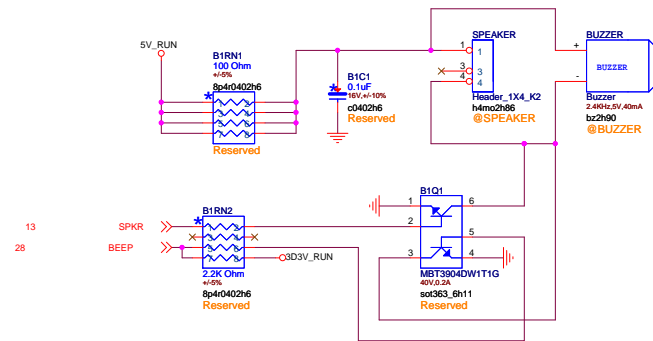
Front Audio



MONO OUT

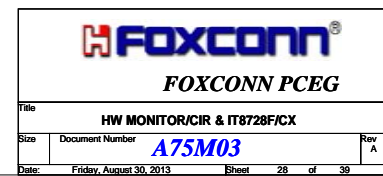


BUZZER/BUZZER Header

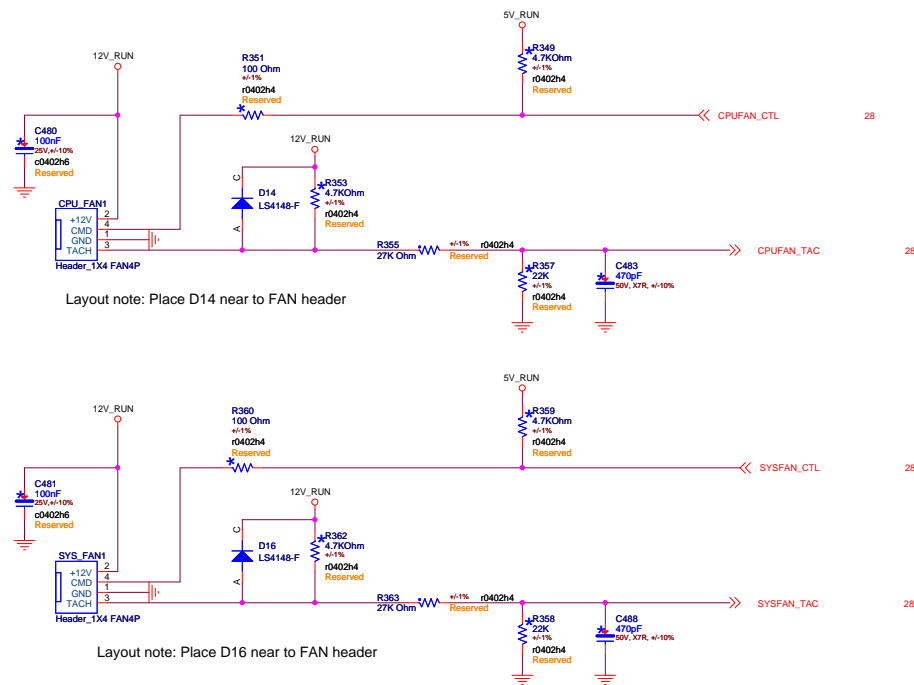


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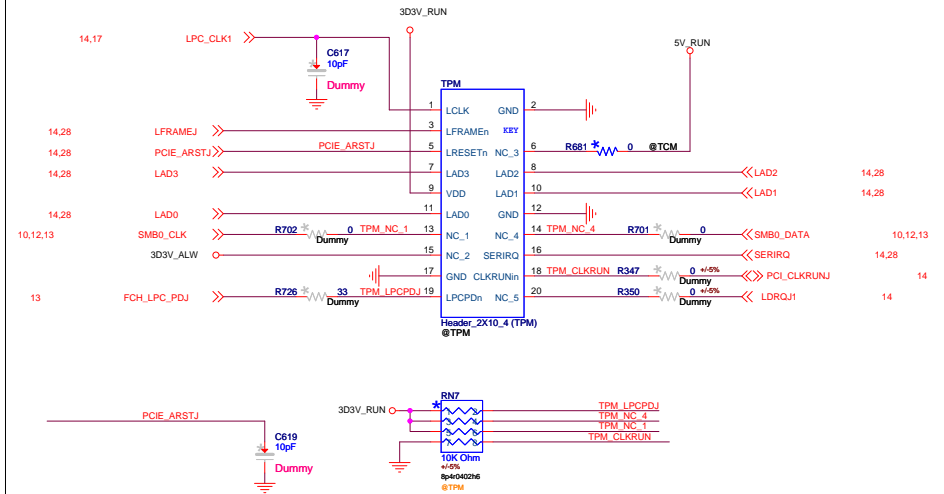
	Symbol	value	Description
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 126		0	K8 power sequence function is enabled
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin 122		0	Enable WDT to rest PWROK
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 80h
		10	The default value of EC Index 15h/16h/17h is Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 40h



FAN



TPM



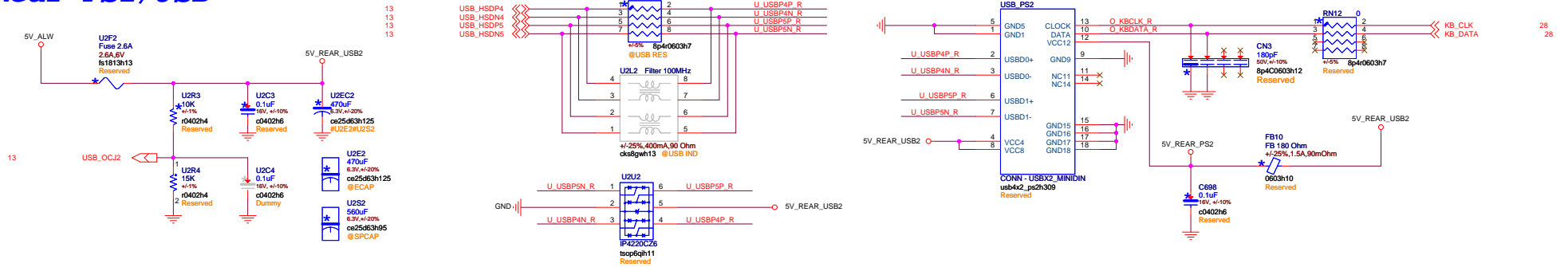
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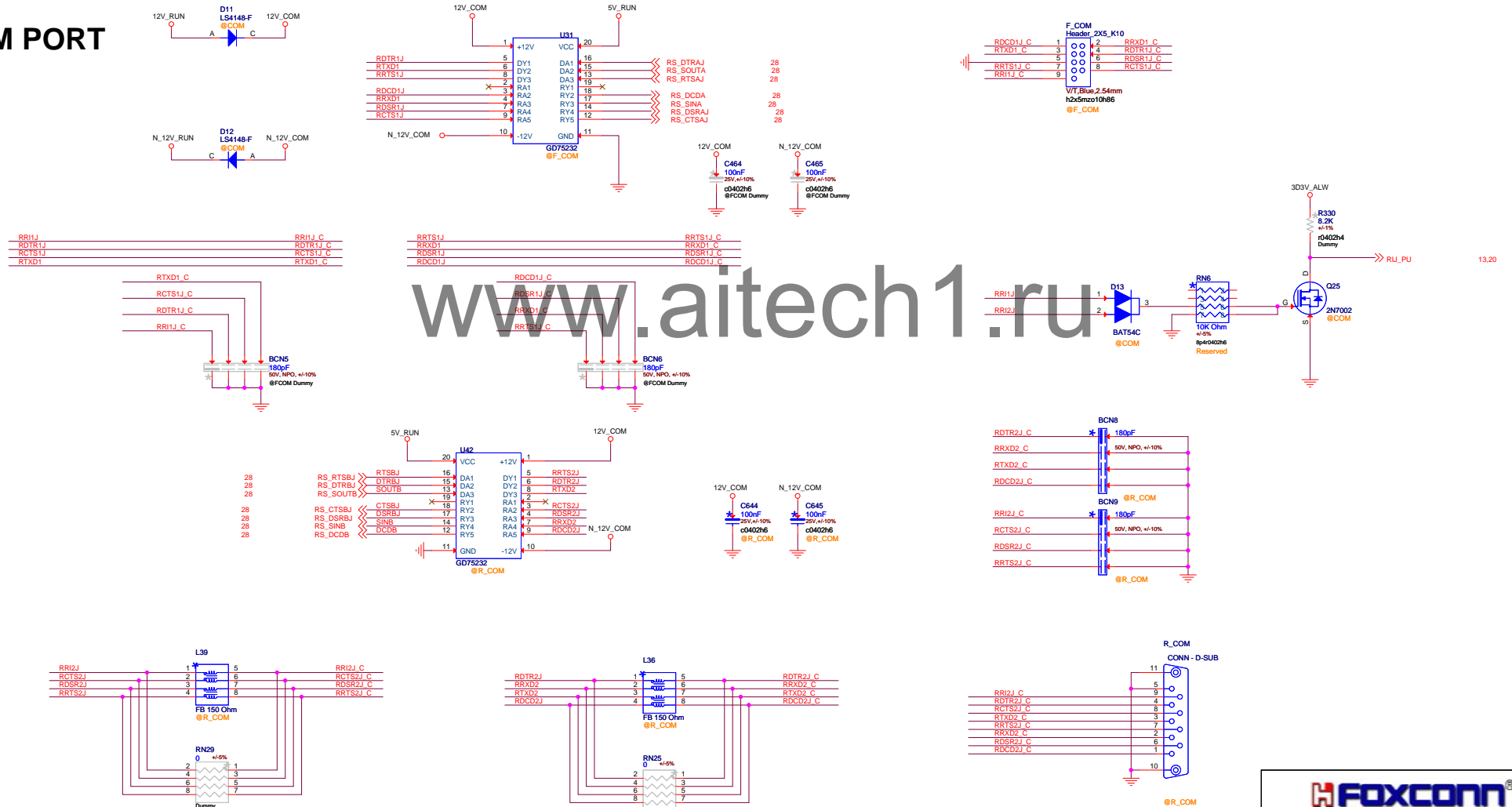
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Title			
FAN & COM & TPM HEADER			
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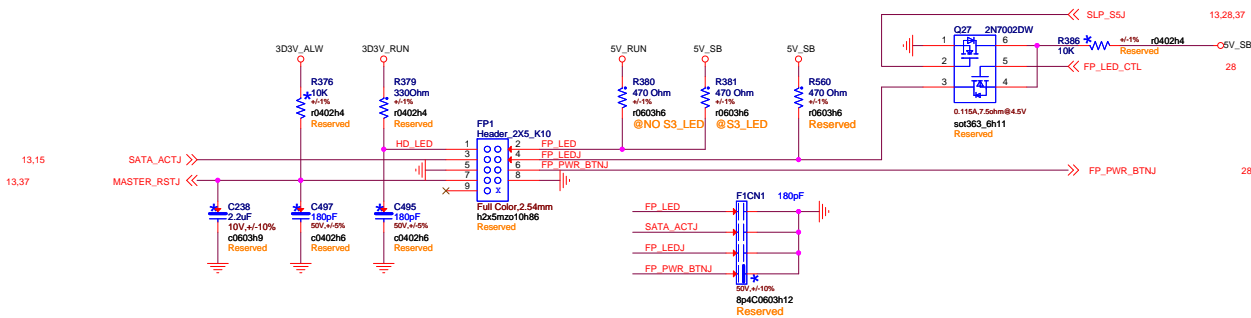
Rear PS2/USB



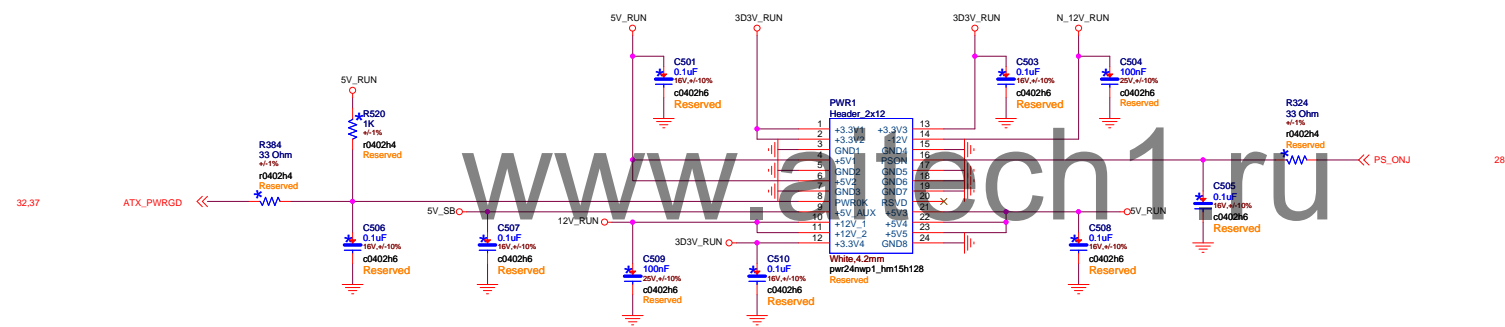
COM PORT



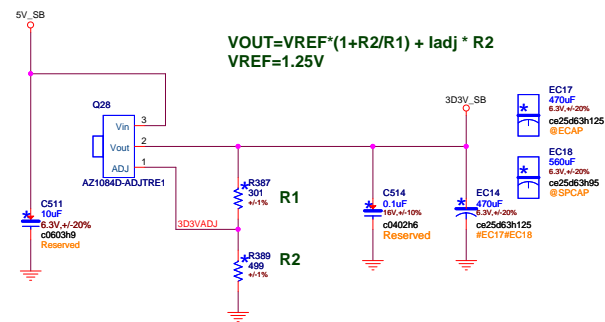
FRONT PANEL HEADER



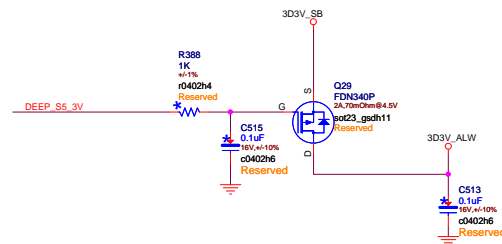
24 PIN ATX CONNECTOR



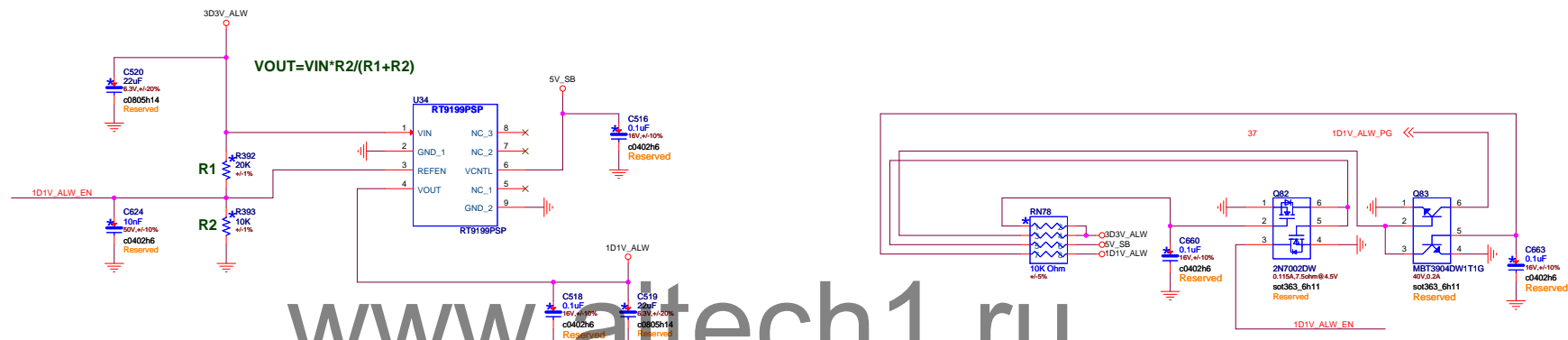
3D3V_SB



3D3V_ALW

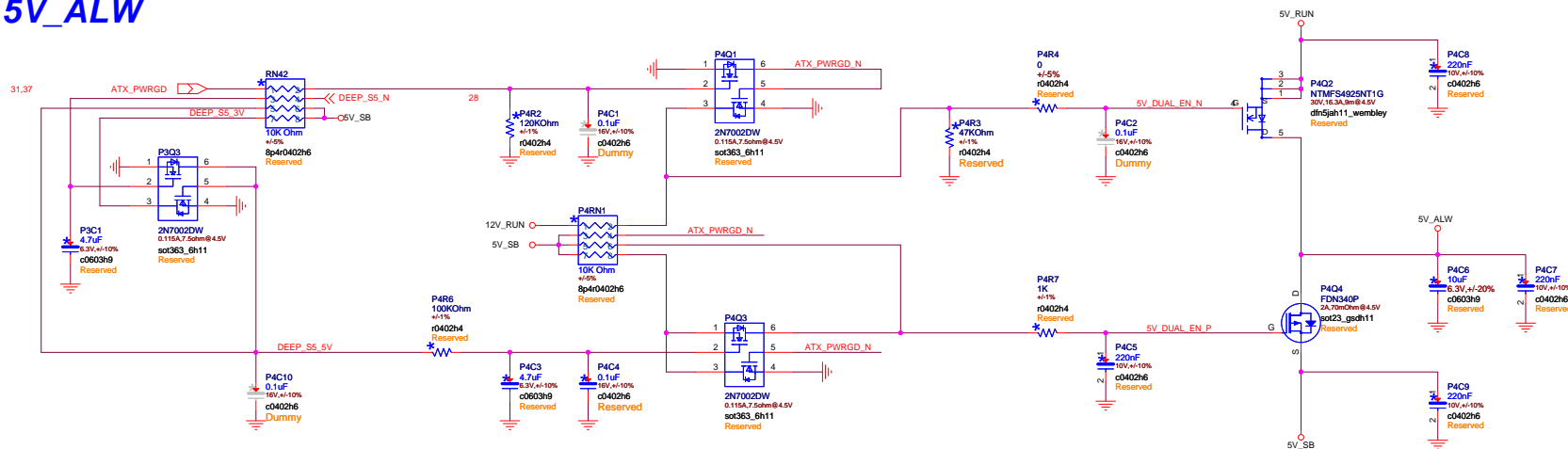


1D1V_ALW



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5V_ALW

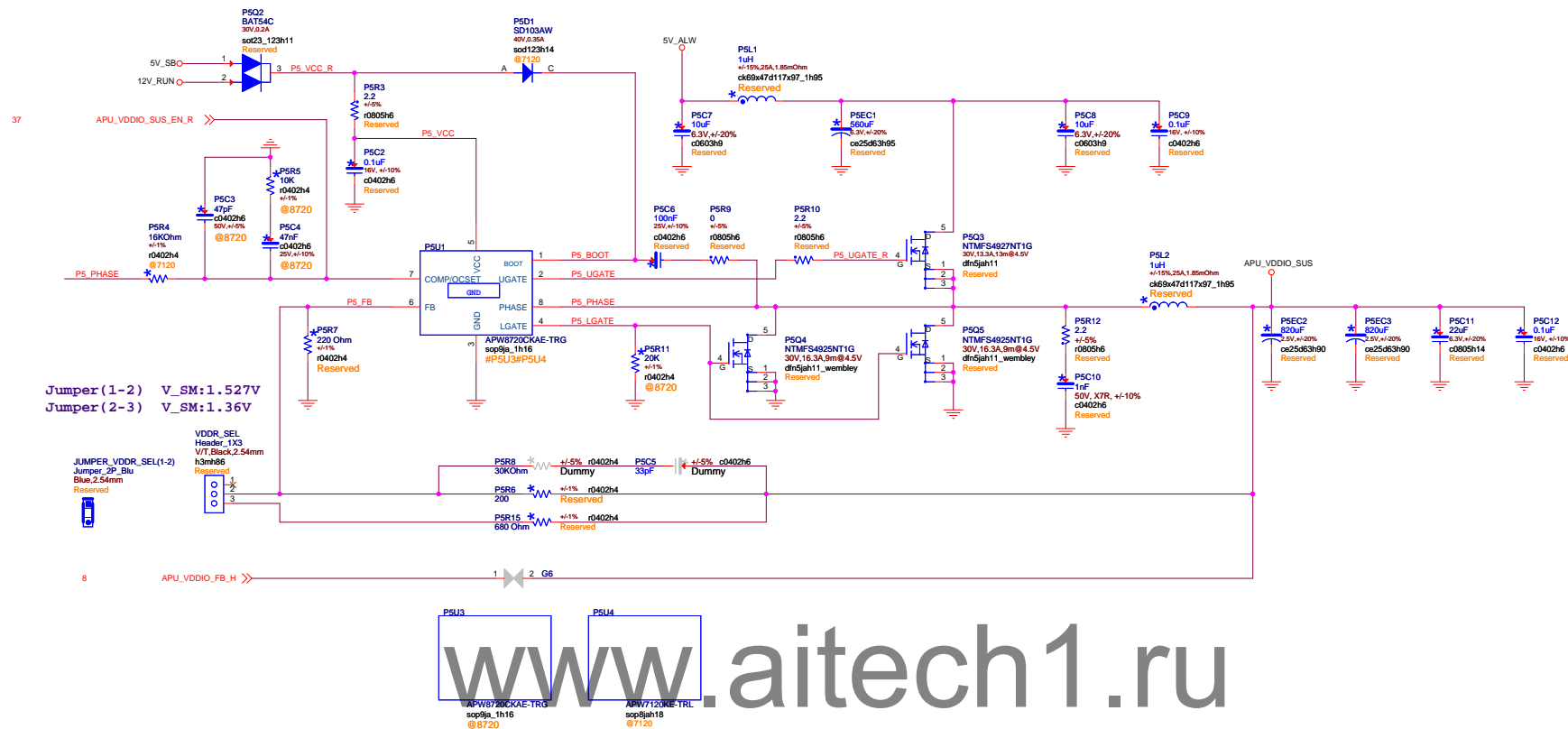


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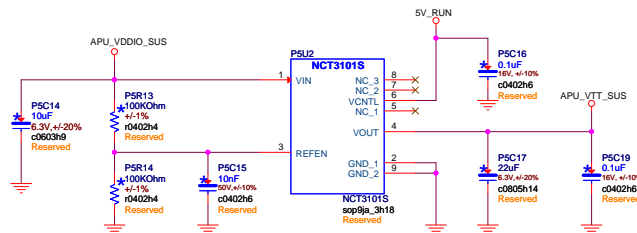
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APU_VDDIO_SUS



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APU_VTT_SUS



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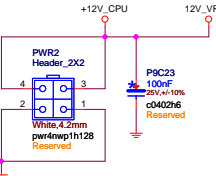
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PWR DDRIII MEMORY

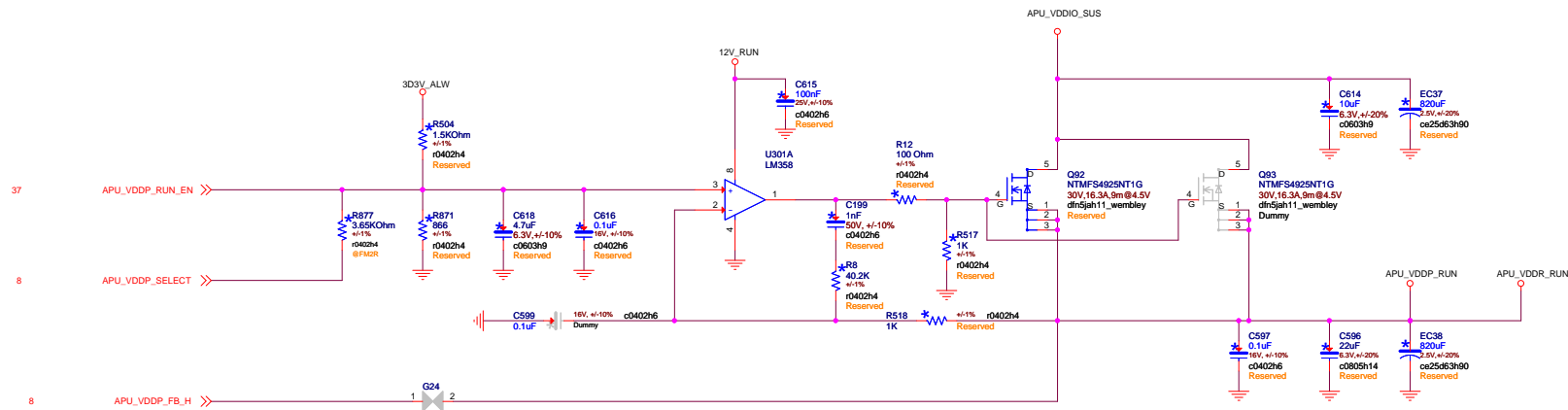
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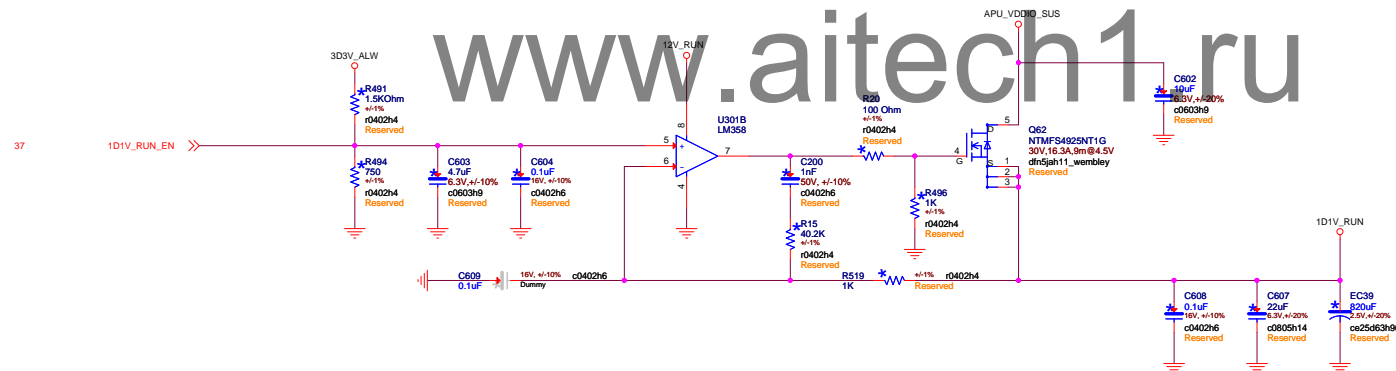
COUT=820*3=2460pF	COUT=820*3=2460pF
ESR=7m/6=1.17m ohm	ESR=7m/3=2.33m ohm
FESR=27.7kHz	FESR=27.8kHz
Fz=150kHz	Fz=40kHz
RLL=1.3m ohm	RLL=4m ohm
AR57=10k	AR57=10.5k
AR68=22.62k	AR68=33k
AC122=212.8 pF	AC122=146 pF
AC133=106 pF	AC135=390 pF



APU_VDDP_RUN



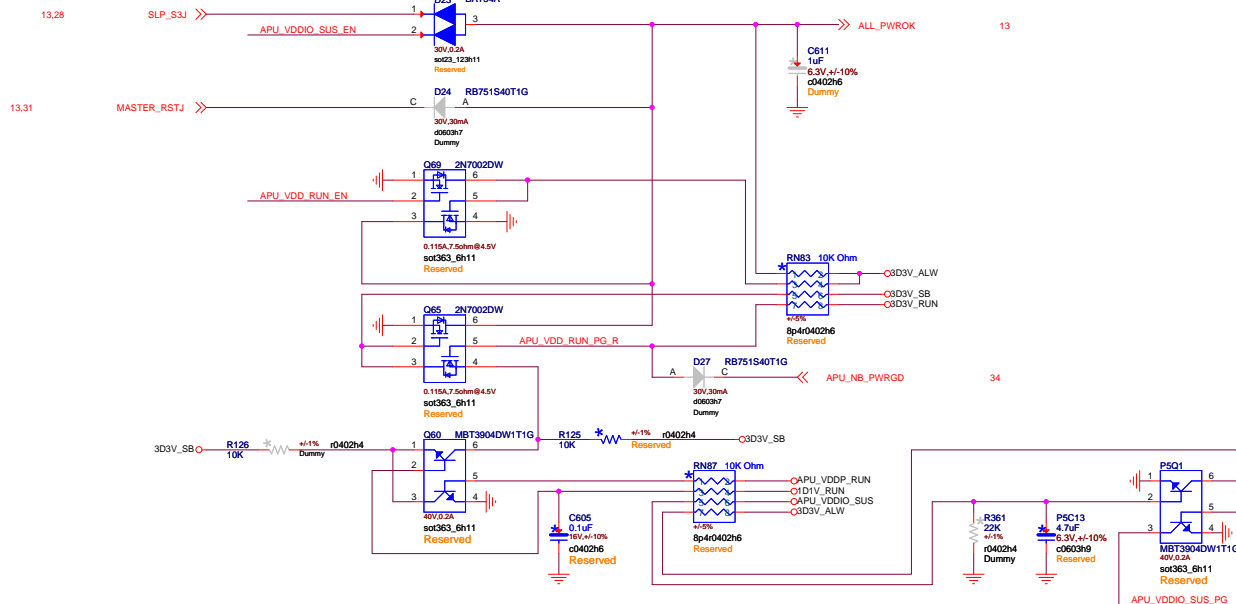
1D1V_RUN

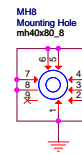
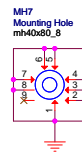
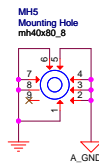
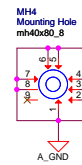
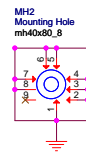


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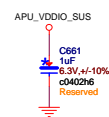
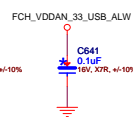
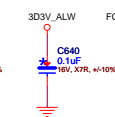
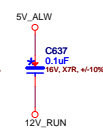
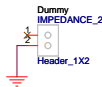
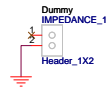
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PWR VDDP/VDDR & 1D1V_RUN			
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ALL POWER GOOD CIRCUIT





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